

Quasi-free-standing monolayer and bilayer graphene growth on homoepitaxial on-axis 4H-SiC(0001) layers

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We demonstrate controlled growth of quasi-free standing monolayer and bilayer graphene on homoepitaxial layers of 4H-SiC using conventional SiC Hot-wall CVD reactor. Such structures may have applications in back gated and in dual gated field effect transistors to open bandgap in bilayer graphene system [1]. Nominally on-axis (with unintentional off-cut of 0.05°) semi-insulating 4H-SiC with Si-face chemomechanically polished were used as substrates (16x16 mm² pieces). SiC growth was then performed under optimized growth parameters for on-axis homoepitaxy, resulting in 100% 4H-SiC polytype in the epitaxial layer [2]. The 4H-SiC epitaxial layers were about 2-3 μm thick with controlled n-type doping of $1 \times 10^{16} \text{ cm}^{-3}$. In order to obtain quasi-free-standing monolayer graphene, only the carbon buffer layer was grown, whereas when bilayer graphene was aimed the growth conditions were optimized to obtain monolayer graphene on the surface of homoepitaxial 4H-SiC layer. Subsequent hydrogen intercalation was performed in order to convert the carbon buffer layer into quasi-free-standing monolayer, and the monolayer graphene into quasi-free standing bilayer graphene. The whole growth process including substrate surface preparation, on-axis homoepitaxial growth, graphene growth and intercalation process can be performed in a single sequence without exposing the sample to air.

The surface morphology of homoepitaxial layers and graphene was observed using optical microscope while the surface step structure was studied using atomic force microscope in tapping mode. 4H polytype in the epilayer was confirmed using the low temperature photoluminescence mapping on random areas, which did not show any foreign polytype inclusions. Several characterization techniques were used to assess the grown graphene. In case of graphene grown on semi-insulating substrate, the sheet resistance and the charge-carrier mobility were estimated using a contactless measurement technique. In addition, the number of graphene layers was determined on random areas of the samples by reflectance mapping using a common micro-Raman spectrometer [3]. Raman mapping was employed in parallel with the reflectance mapping, thus confirming the number of layers inferred by the reflectance mapping alone, but also yielding additional information on the stress conditions and the doping of the grown graphene. Fig. 1 illustrates examples of reflectance maps of samples with predominantly monolayer (Fig.1a) and bilayer (Fig.1b) graphene together with typical Raman spectra obtained from the corresponding regions. Different positions in several samples were mapped using both above-mentioned techniques to obtain an overview of the thickness uniformity and quality of graphene over large areas. Hall bar structures are also fabricated on these layers with the aim of studying the electronic properties of monolayer and bilayer graphene.

It is well known that under standard growth conditions epitaxial growth on the *on-axis* Si-face of 4H-SiC does not produce 100% 4H polytype in the epilayer, but leads to the formation of 3C-SiC inclusions together with other defects in the epilayer. In this work we will present also our unique growth process designed for reproducible homoepitaxial growth of 100% 4H-SiC polytype in the epilayer on on-axis substrate. The epilayer surface morphology is investigated as well and appears to be relatively rougher compared to the substrate, which is mainly due to step-bunching on the Si-face along with different growth mechanism on on-axis substrate. In the case of off-cut substrates (e.g., 4° or 8° off-cut) the epitaxial growth is driven by step-flow growth, while in the case of on-axis substrates the growth can be a mixture of step and spiral growth which together with step-bunching leads to rougher surface. However, it is possible to further optimize the growth process to reduce the surface roughness. As-grown epilayer surface shows relatively wide terraces covered with micro-steps of 0.5 to 1 nm height between macro-steps of few tens of nm height (Fig. 2, left image). Graphene growth on such surface does not seem to alter the macro-step structure, however; micro-steps coalesce to form relatively large steps of 2-3 nm leaving atomically flat wide terraces (Fig.2, right image). Additionally, the macro-steps are not steep (as in the case of step-bunching on substrate when exposed to high temperature) and laterally extend

over large distances of over 100 μm depending on the epilayer thickness. Device implementation on such samples taking into account the features of the surface morphology will also be discussed.

References

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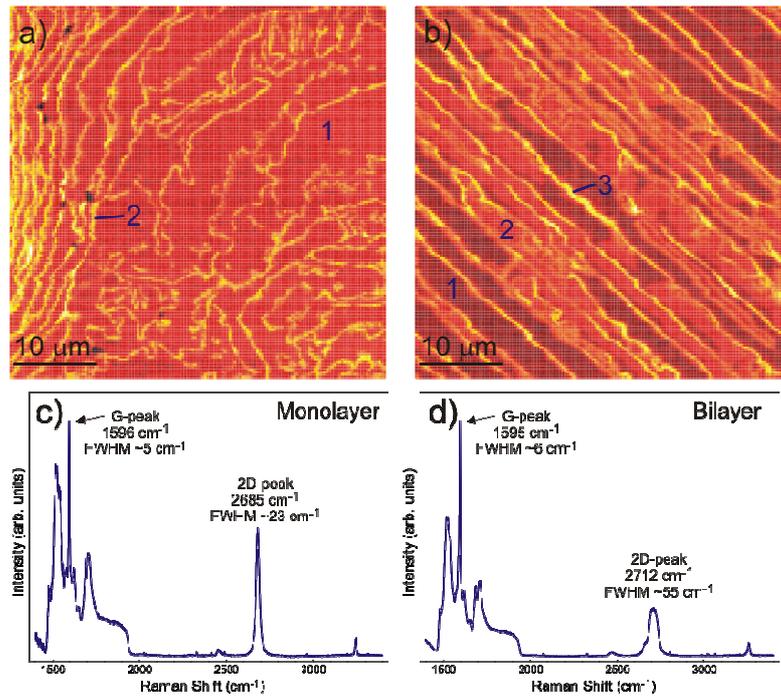


Fig. 1 Fig. 1. Reflectance maps showing predominantly (a) monolayer graphene, and (b) bilayer graphene. The number of layers (colour-coded) is denoted on the sample. (c) and (d) display Raman spectra obtained from the sample with monolayer and sample with bilayer regions, respectively.

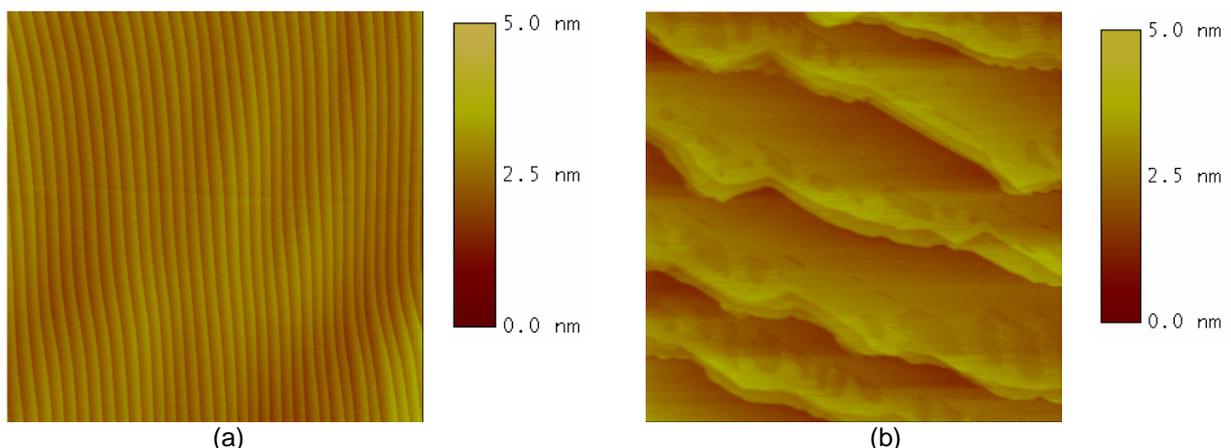


Fig. 2 AFM image taken from (a, $20 \times 20 \mu\text{m}^2$) as-grown epilayer surface covered with 1 nm height steps and (b, $5 \times 5 \mu\text{m}^2$) after graphene growth. The micro-step structure on as-grown epilayer surface (a) coalesces to form relatively larger steps and wider terraces after graphene growth (b).